METHOD FOR DETERMINING SEMICONDUCTOR OVERLAY ON GROUNDRULE DEVICES

ABSTRACT OF THE DISCLOSURE

A method of determining overlay error comprises creating a first and second layers of an integrated circuit, each having an active circuit feature and an adjacent kerf area. Each kerf area includes a first measurement feature separated from and corresponding substantially to the layer's active circuit feature. The circuit and kerf areas of the layers are substantially superimposed. The distance of separation between the active circuit feature and the layer kerf measurement feature in each layer in the direction of overlay error is the same. The second layer kerf measurement feature is displaced from the first layer kerf measurement feature in a direction perpendicular to the direction that the overlay error is to be determined. Overlay error is determined by measuring distance of separation in the direction of overlay error between the common points of reference of each of the first and second layer kerf measurement features.